

Ser. No. 09/716,721  
Internal Docket No. PU000125  
Customer No. 24498

**IN THE CLAIMS**

1. (Currently amended) A serial compressed bus interface for interfacing with a bus having a single serial data line and at least one control line, comprising:

a serial-to-parallel converter having a ~~single serial data~~ input coupled to said signal serial data line and adapted to receive time-division multiplexed serial data from a plurality of data sources, and said serial-to-parallel converter having a plurality of parallel output lines for providing thereon a packets of said time-division multiplexed serial data in parallel form to ~~one of~~ a plurality of devices associated with data applications; and

enable logic having an input coupled to said at least one control line for receiving a ~~coupled to each of said plurality of devices and adapted to provide at least one~~ data valid signal that identifies which of said plurality of devices is associated with a particular packet of the time-division multiplexed serial data, said enable logic deriving a signal from said data valid signal to enable said identified device to receive said particular packet in parallel form, as provided by said serial-to-parallel converter.

2. (Cancelled)

3. (Previously presented) The serial compressed bus interface according to claim 1, further comprising a request control circuit adapted to output at least one request signal that requests the time-division multiplexed serial data for at least one of the plurality of devices associated with data applications.

4. (Canceled)

Ser. No. 09/716,721  
Internal Docket No. PU000125  
Customer No. 24498

5. (Previously presented) The serial compressed bus interface according to claim 3, wherein the request control circuit is further adapted to encode the at least one request signal to correspond to more than one of the plurality of devices associated with data applications.

6. (Currently amended) A method for transmitting serial compressed data from a plurality of data sources via a bus having a single data line and at least one control line to a plurality of devices associated with data applications, comprising the steps of:

time-division multiplexing the serial compressed data from the plurality of data sources to generate time-division multiplexed serial compressed data comprising packets onto a said single data line;

providing to said at least one control line at least one data valid signal that identifies which of said plurality of devices is associated with a particular one of said packets;

converting said particular one of said packets ~~the time-division multiplexed serial compressed data~~ to a packet of parallel data, and outputting said packet of parallel data for receipt by said identified device ~~at least one of said plurality of devices associated with data applications; and~~

providing receiving from said at least one control line said at least one data valid signal that identifies which of said plurality of devices is associated with said outputted packet of parallel data; and

deriving a signal from said at least one data valid signal to enable said identified device to receive said outputted packet of parallel data.

7. (Canceled)

Ser. No. 09/716,721  
Internal Docket No. PU000125  
Customer No. 24498

8. (Previously presented) The method according to claim 6, further comprising the step of encoding a data valid signal to indicate that the time-division multiplexed serial compressed data is valid for more than one of said devices associated with data applications.

9. (Previously presented) The method according to claim 6, further comprising the step of encoding a request signal to indicate that the time-division multiplexed serial compressed data is requested by more than one of the devices associated with data applications.

10. (Canceled)

Ser. No. 09/716,721  
Internal Docket No. PU000125  
Customer No. 24498  
**Remarks/Arguments**

Claims 1, 3-6, 8 and 9 are pending. Claims 1 and 6 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over Swenson (United States Patent No. 5,926,120) in view of Zaun (United States Patent Publication No. 2002/0024610). Claims 3, 4, 5, 8 and 9 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over Swenson in view of Zaun, and further in view of Pannell (United States Patent No. 6,636,483).

Claims 1 and 6 are amended. Claim 4 is canceled without prejudice and disclaimer.

Applicants respectfully disagree that the combination of IP control logic 202 and other downstream components such as data MUX 210 in Zaun should be interpreted as the enable logic in the Advisory Action for the following reasons. FIG. 2 shows the details of each of a plurality of input processors 120, and each input processor 120 accepts a different serial input stream and delivers a packet to a different buffer 104 when the packet is valid. Thus, if we interpret each input processor 120 (except the serial to parallel converter 200) as the enable logic, the enable logic does not couple to a plurality of devices as required by claim 1 because each input processor 120 is associated with only one buffer 104 (relied upon as a device). Furthermore, claim 1 recites a bus interface. As such, the enable logic should directly couple to the bus as well. The IP control logic 202 (relied upon as part of the enable logic), however, is coupled to the INFOBUS (relied upon as the serial compressed bus) through the serial-to-parallel converter 200 (relied upon as the serial-to-parallel converter).

However, in the interest of advancing the prosecution, applicants have amended claims 1 and 6 to more particularly point out and distinctly claim the subject matter that applicants regard as the invention. For example claim 1 recites a serial compressed bus interface for interfacing with a bus having a single serial data line and at least one control line, comprising:

Ser. No. 09/716,721  
Internal Docket No. PU000125  
Customer No. 24498

*a serial-to-parallel converter having a data input coupled to said signal serial data line and adapted to receive time-division multiplexed serial data from a plurality of data sources, said serial-to-parallel converter having a plurality of parallel output lines for providing thereon packets of said time-division multiplexed serial data in parallel form to a plurality of devices associated with data applications; and*  
*enable logic having an input coupled to said at least one control line for receiving a data valid signal that identifies which of said plurality of devices is associated with a particular packet of the time-division multiplexed serial data, said enable logic deriving a signal from said data valid signal to enable said identified device to receive said particular packet in parallel form, as provided by said serial-to-parallel converter.*

Thus, the enable logic receives the data valid signal from the control line of the bus and the serial-to-parallel converter receives the time-division multiplexed serial data from the single serial data line of the bus.

By contrast, the IP control logic 202 (relied upon as the enable logic) receives a valid packet signal (relied upon as the data valid signal) from the PID table 122, which is not part of the INFOBUS (relied upon as the bus), let alone a control line of the INFOBUS.

Furthermore, the enable logic must derive a signal from the received data valid signal to enable the device identified by the data valid signal to receive a particular packet. By contrast, the IP control logic 202 does not derive a signal from the valid packet signal to enable the packet buffer 104 (relied upon as one of the plurality of devices) to receive a packet. The IP control logic 202 simply sends the packet to the packet buffer 104 for storage. See paragraph [0020].

Since, as admitted in the Advisory Action, Swenson also does not disclose or suggest enable logic, amended claim 1, and dependent claims 3 and 5, are patentable over Swenson and Zaun.

Ser. No. 09/716,721  
Internal Docket No. PU000125  
Customer No. 24498

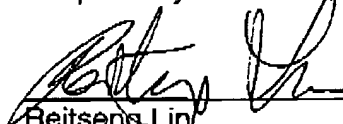
Furthermore, claim 1 recites a serial-to-parallel converter that has a plurality of parallel output lines for providing thereon packets to a plurality of devices. By contrast, the serial-to-parallel converter either in Swenson or Zaun does not provide packets to a plurality of devices. It sends the packet to one device only, such as buffer 104 in Zaun.

Since independent claim 6 is similarly amended, claim 6, and dependent claims 8 and 9, are patentable over Swenson and Zaun for similar reasons discussed above with respect to claim 1.

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. No fee is believed due in regard to the present amendment. However, if a fee is due, please charge the fee to Deposit Account 07-0832. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at 609-734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled.

Respectfully submitted,

By:

  
Reitseng Lin  
Registration No. 42,804  
Phone: 609-734-6813

THOMSON Licensing LLC.  
PO Box 5312  
Princeton, NJ 08543-5312  
Date: January 16, 2007